

Figure 1

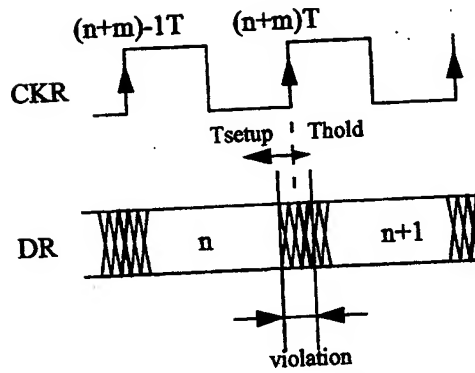


Figure 2

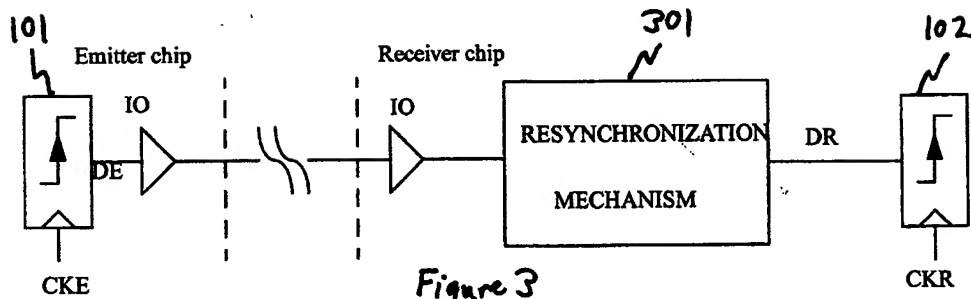


Figure 3

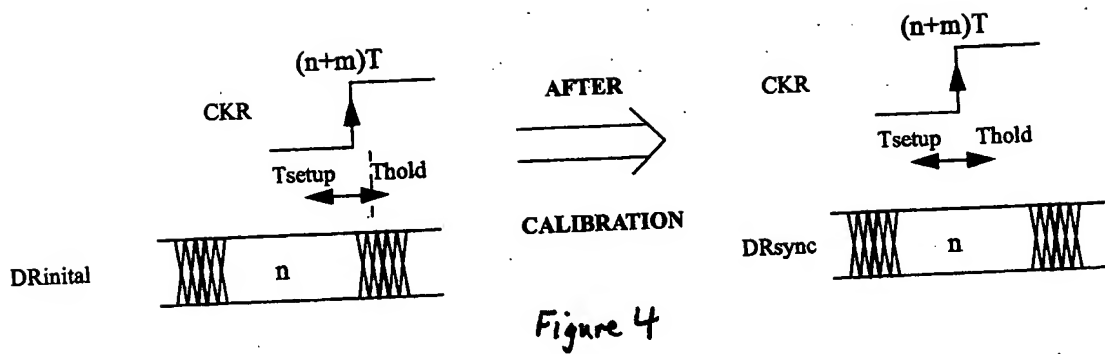


Figure 4

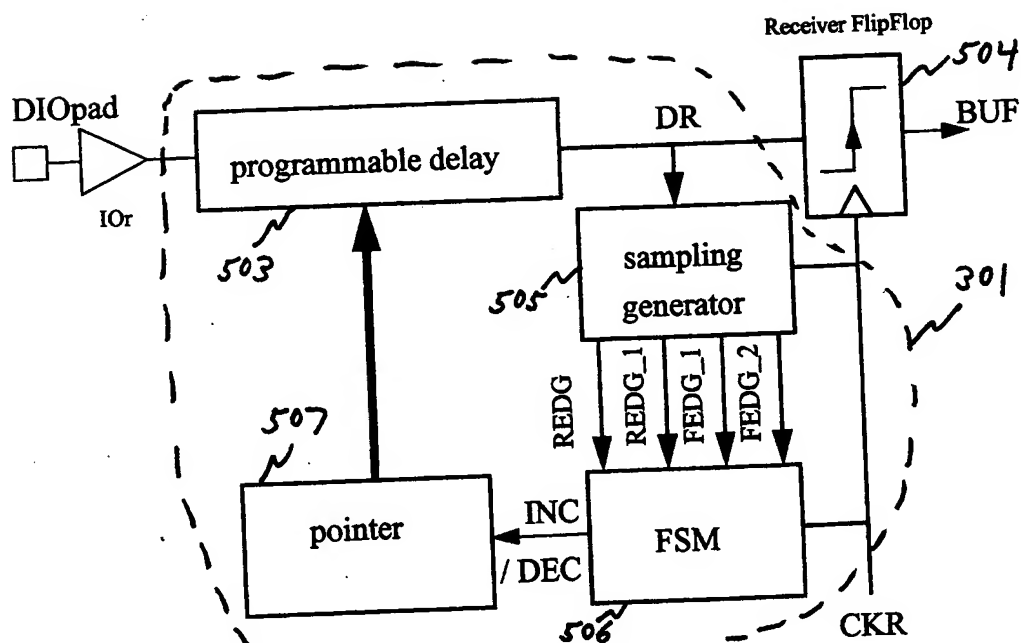


Figure 5

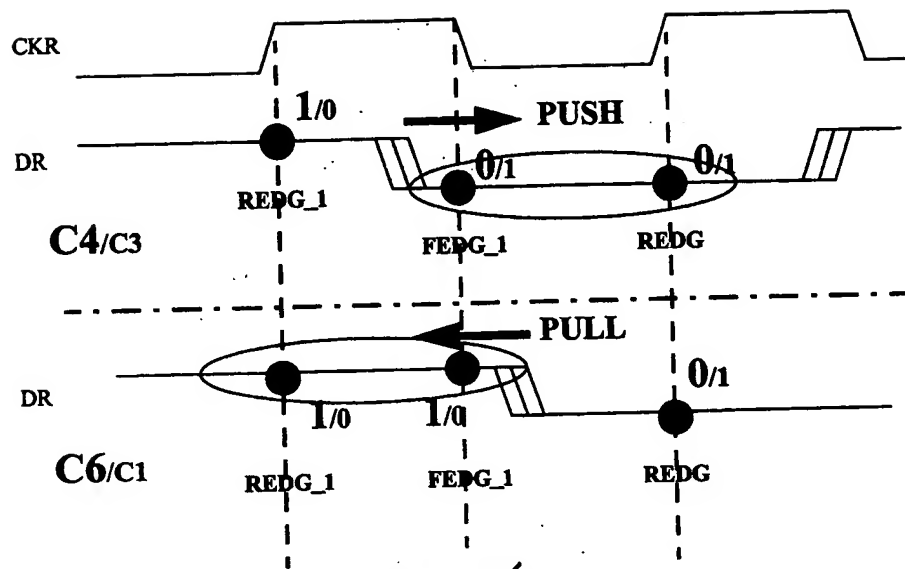


Figure 6

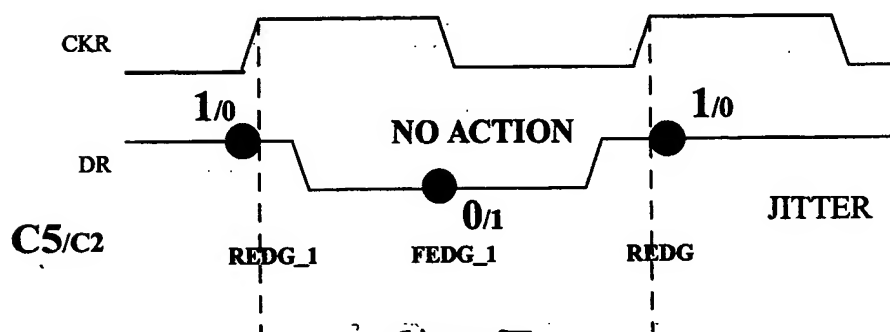


Figure 7

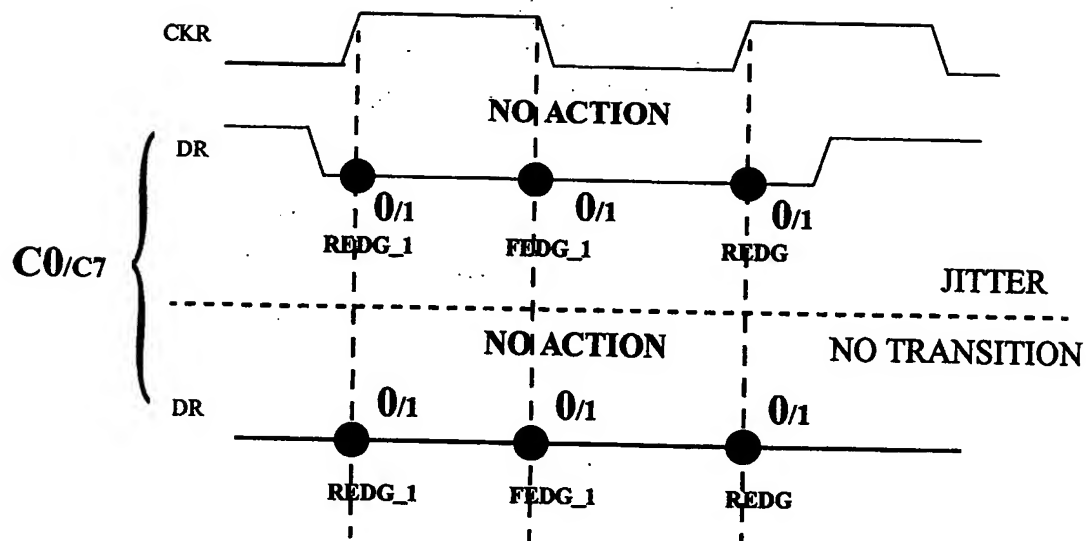


Figure 8

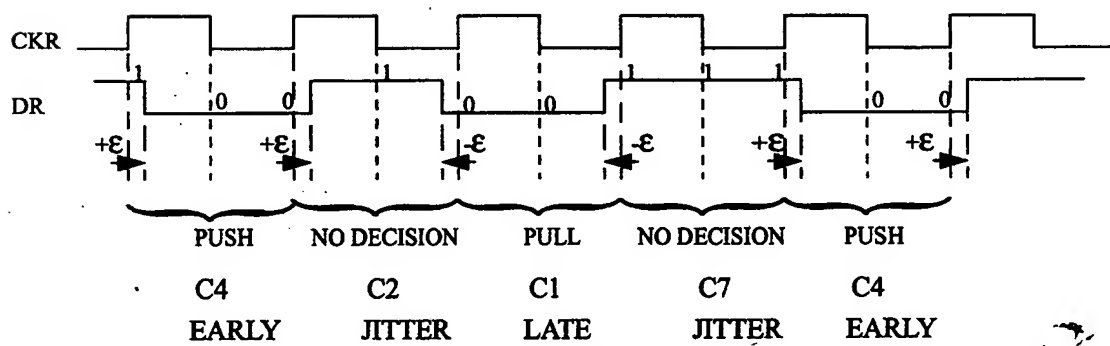


Figure 9

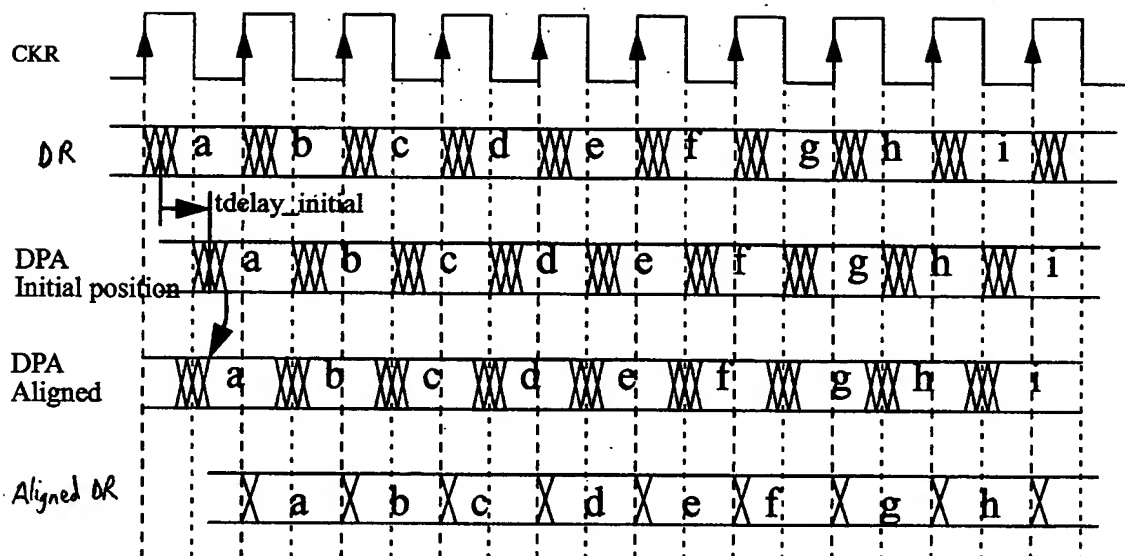


Figure 12

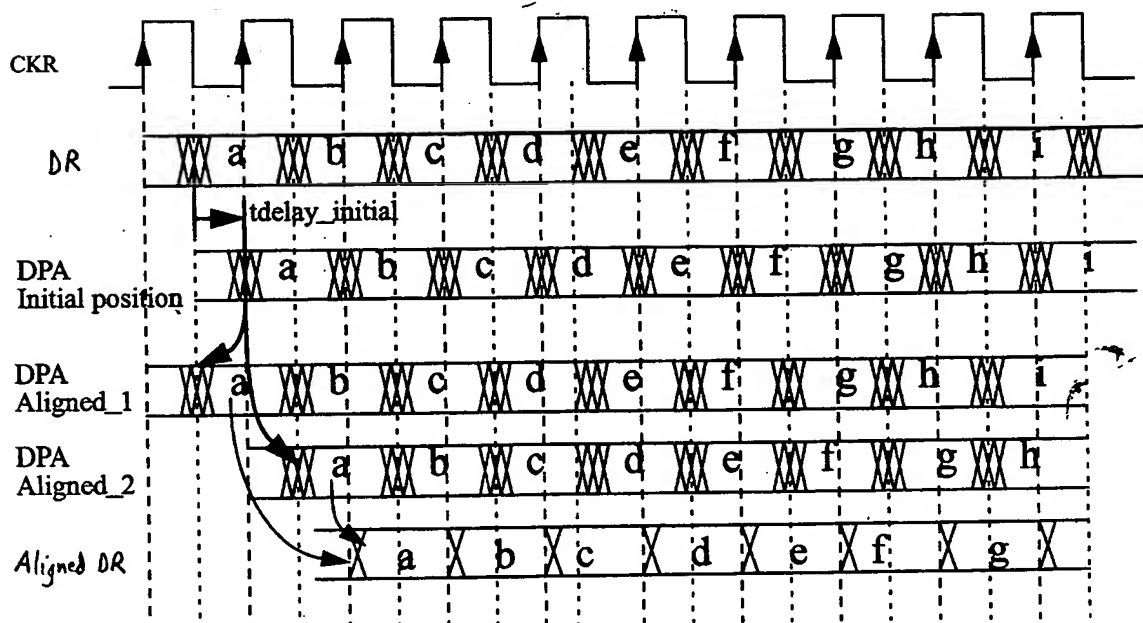


Figure 13

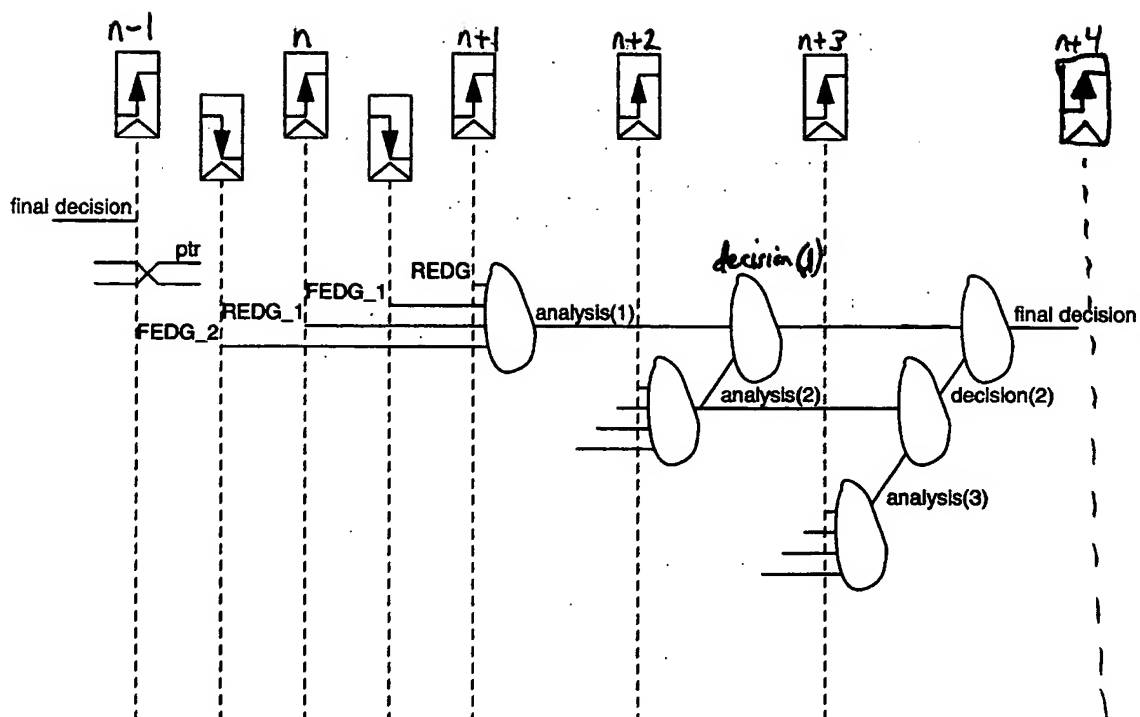


Figure 14

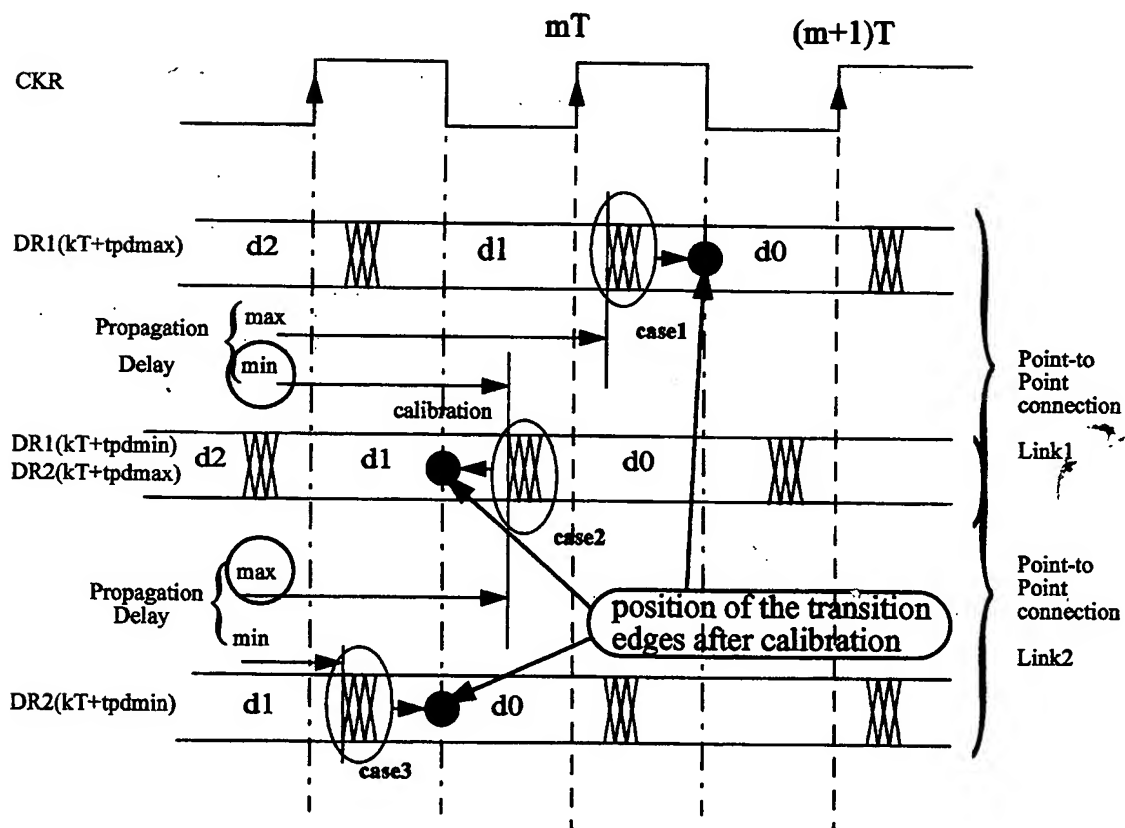


Figure 15

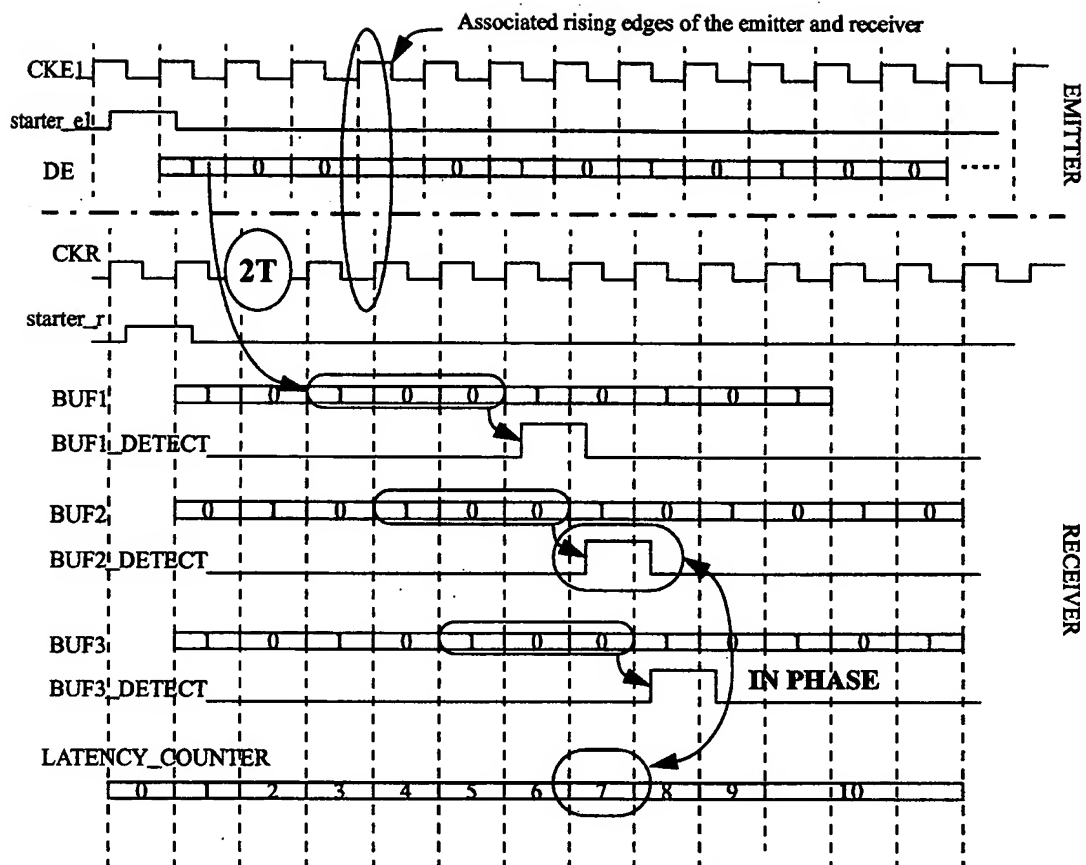


Figure 16

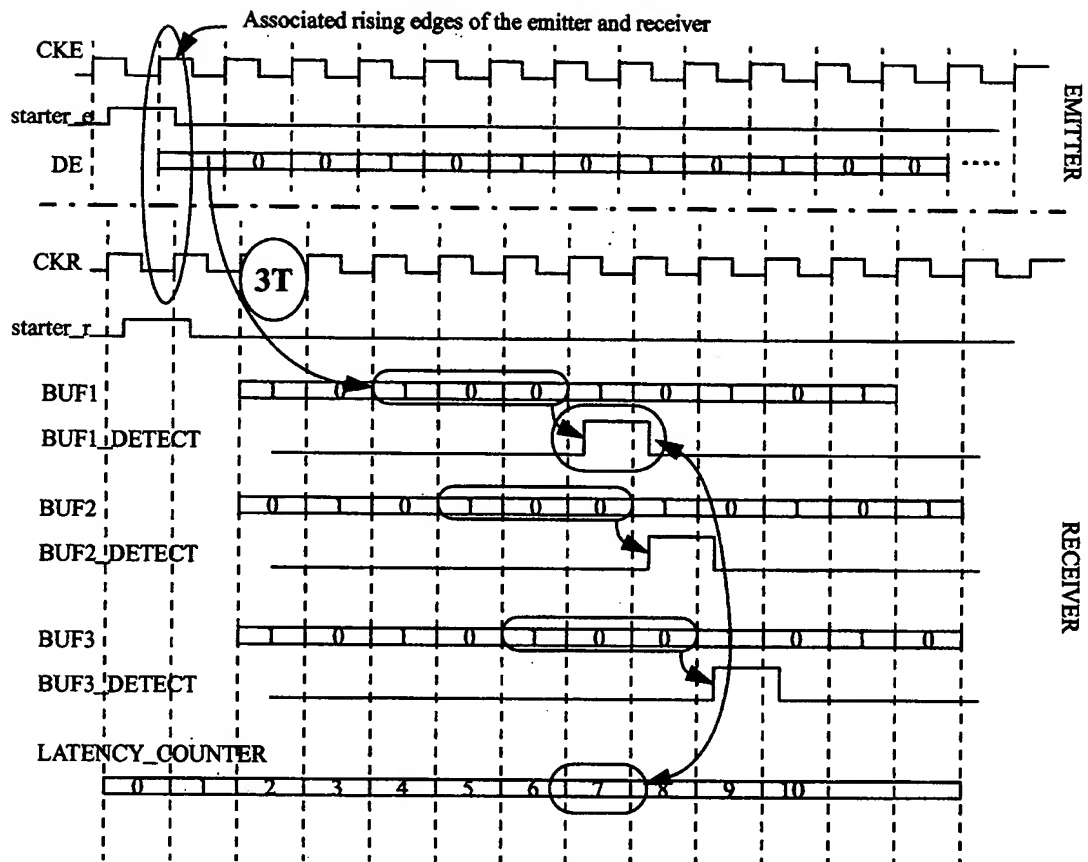
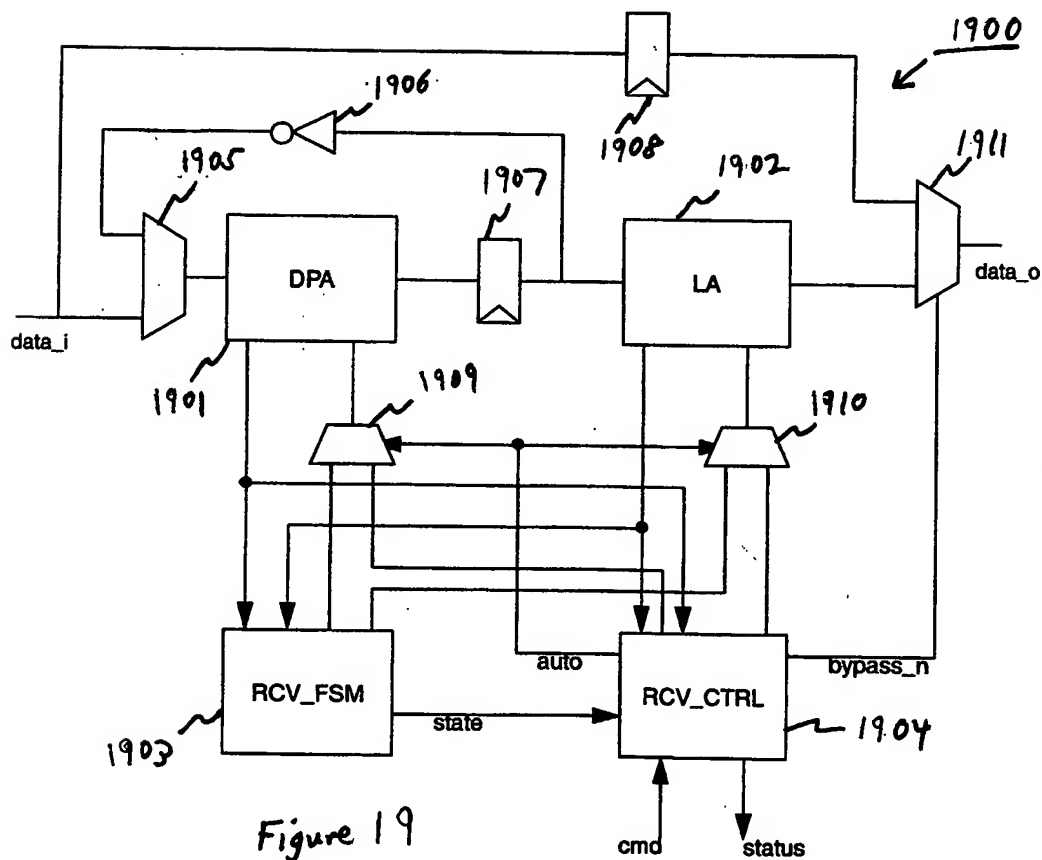
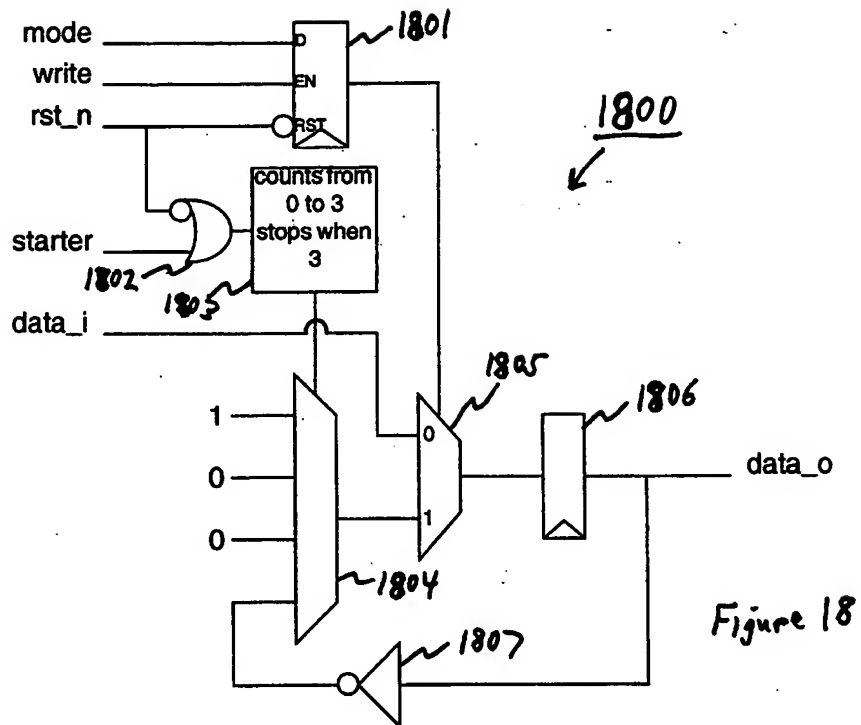
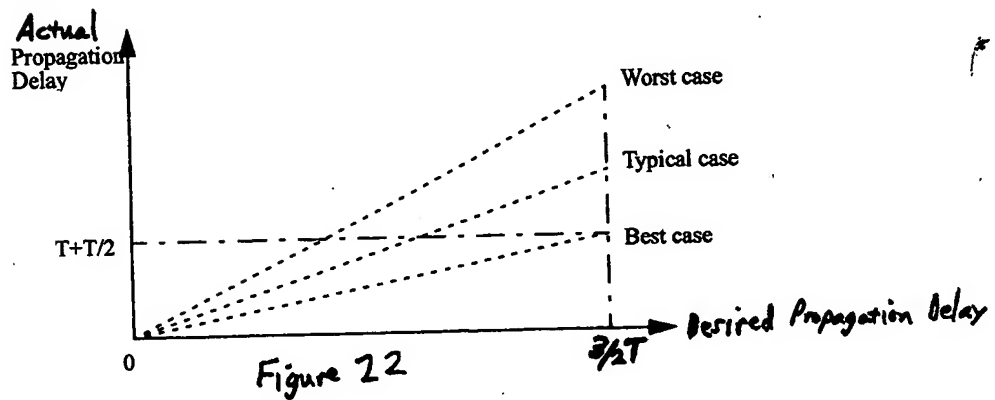
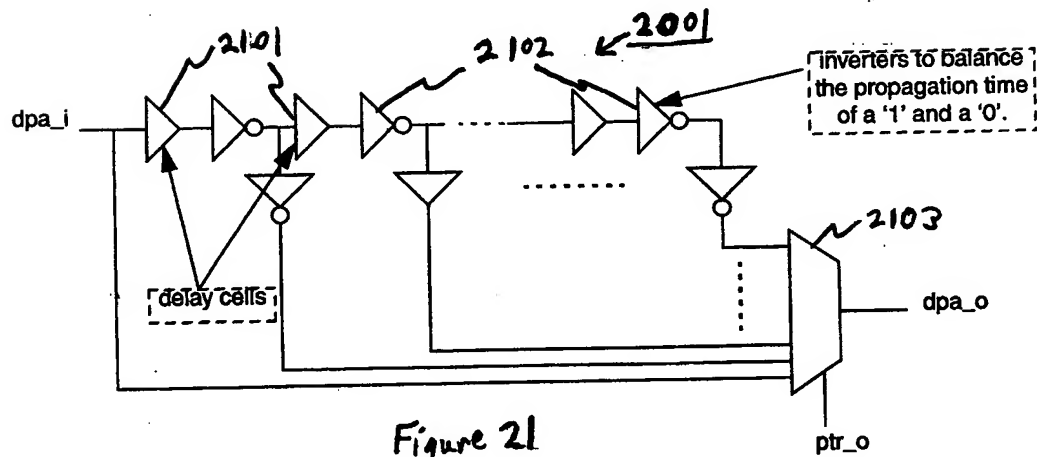
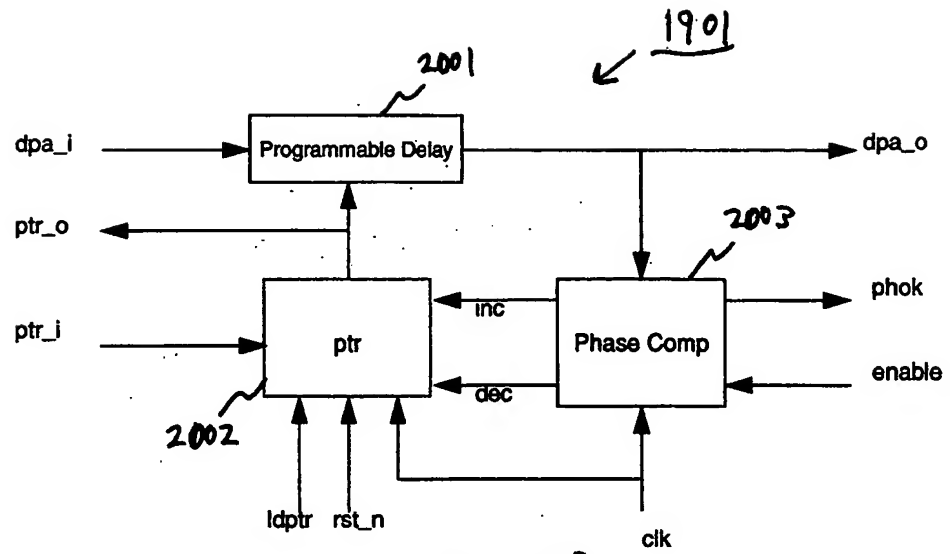


Figure 17





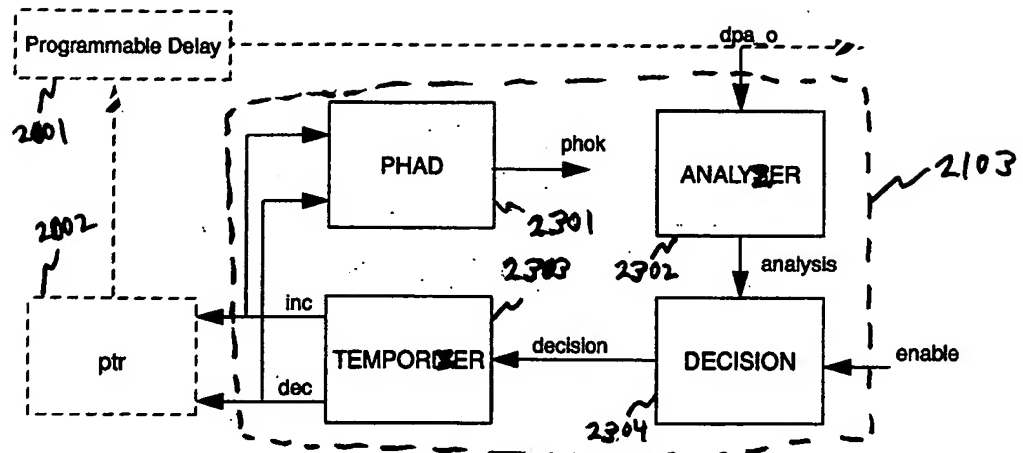


Figure 23

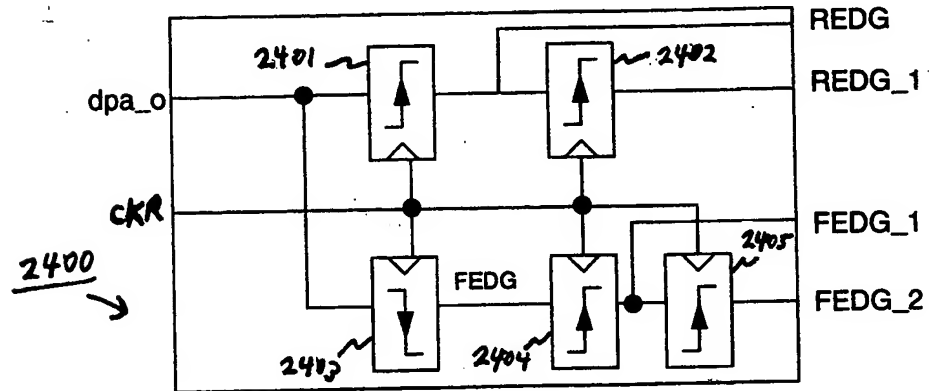


Figure 24

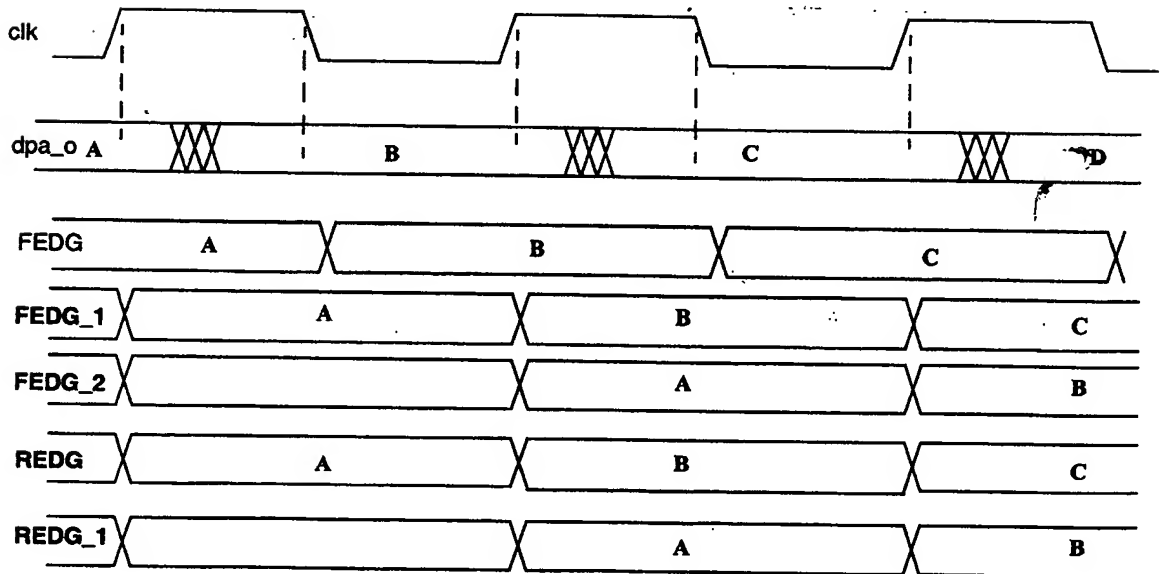
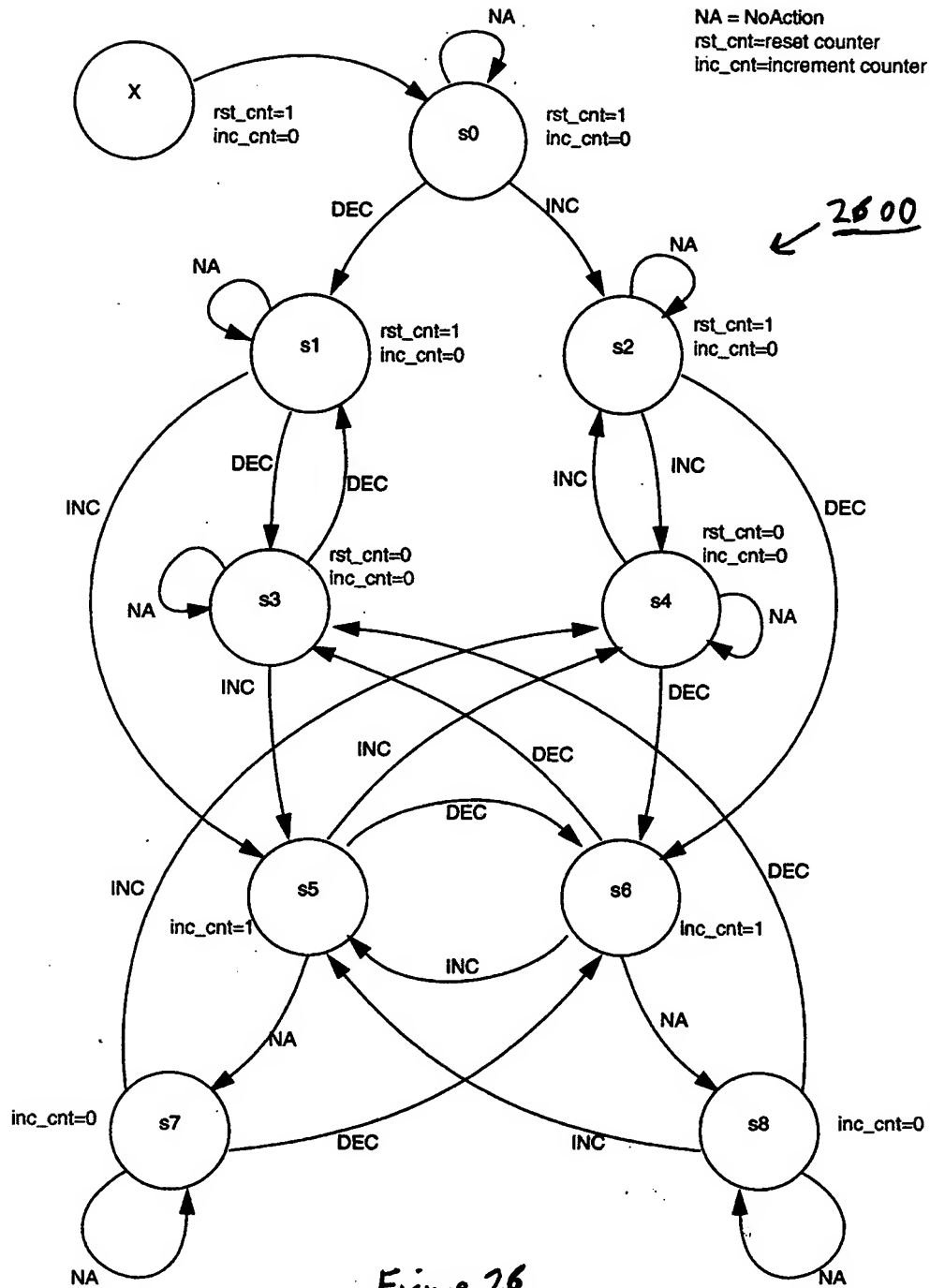


Figure 25



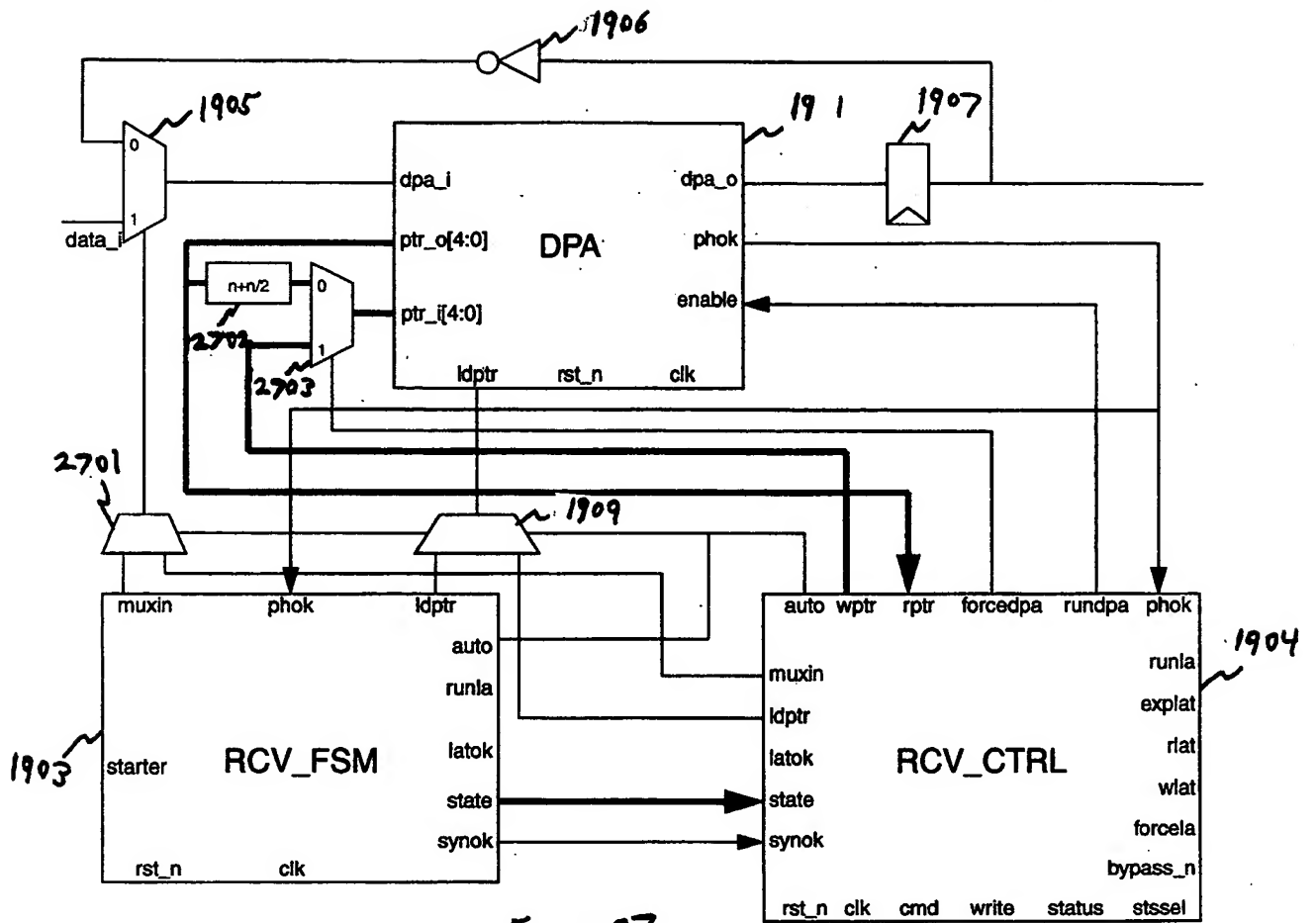


Figure 27

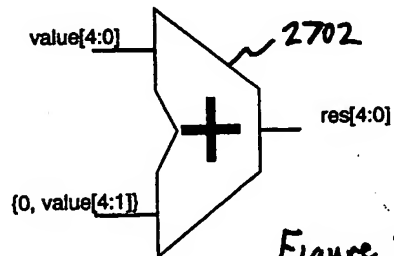


Figure 28

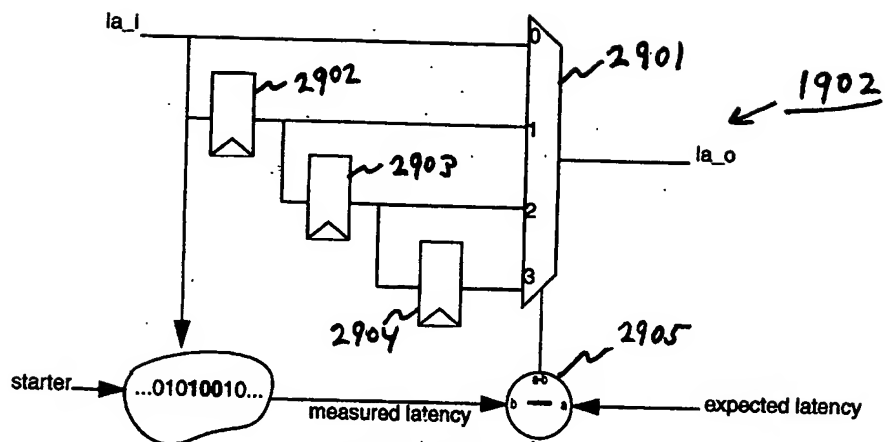


Figure 29

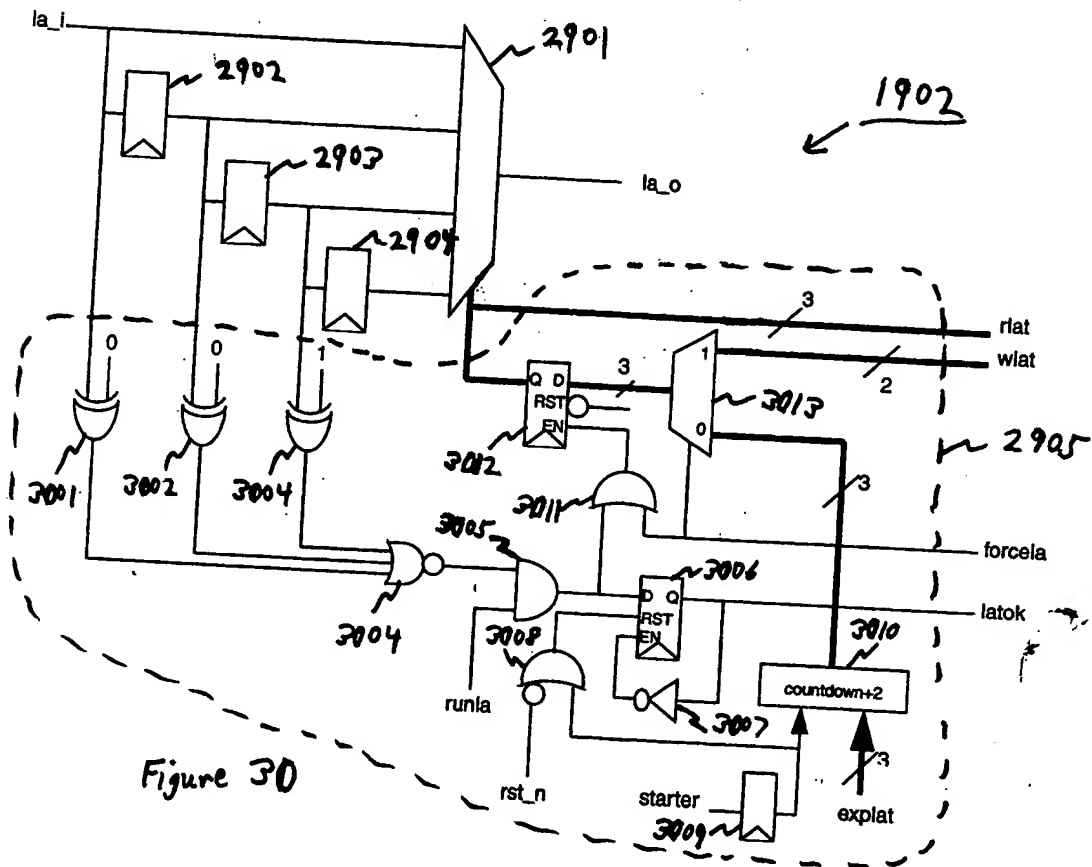


Figure 30

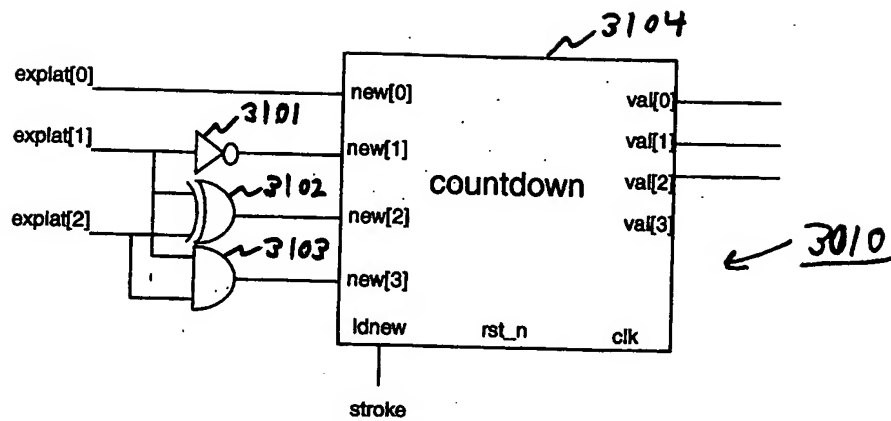


Figure 31

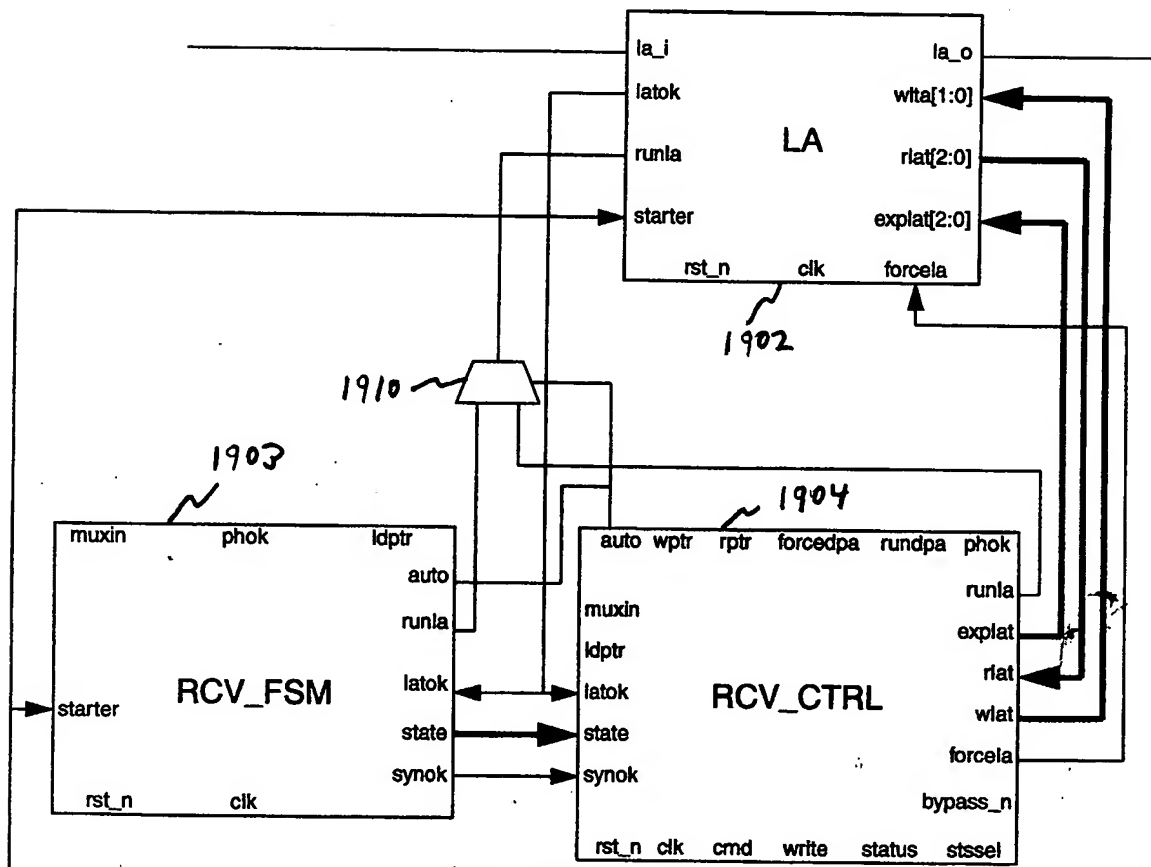


Figure 32

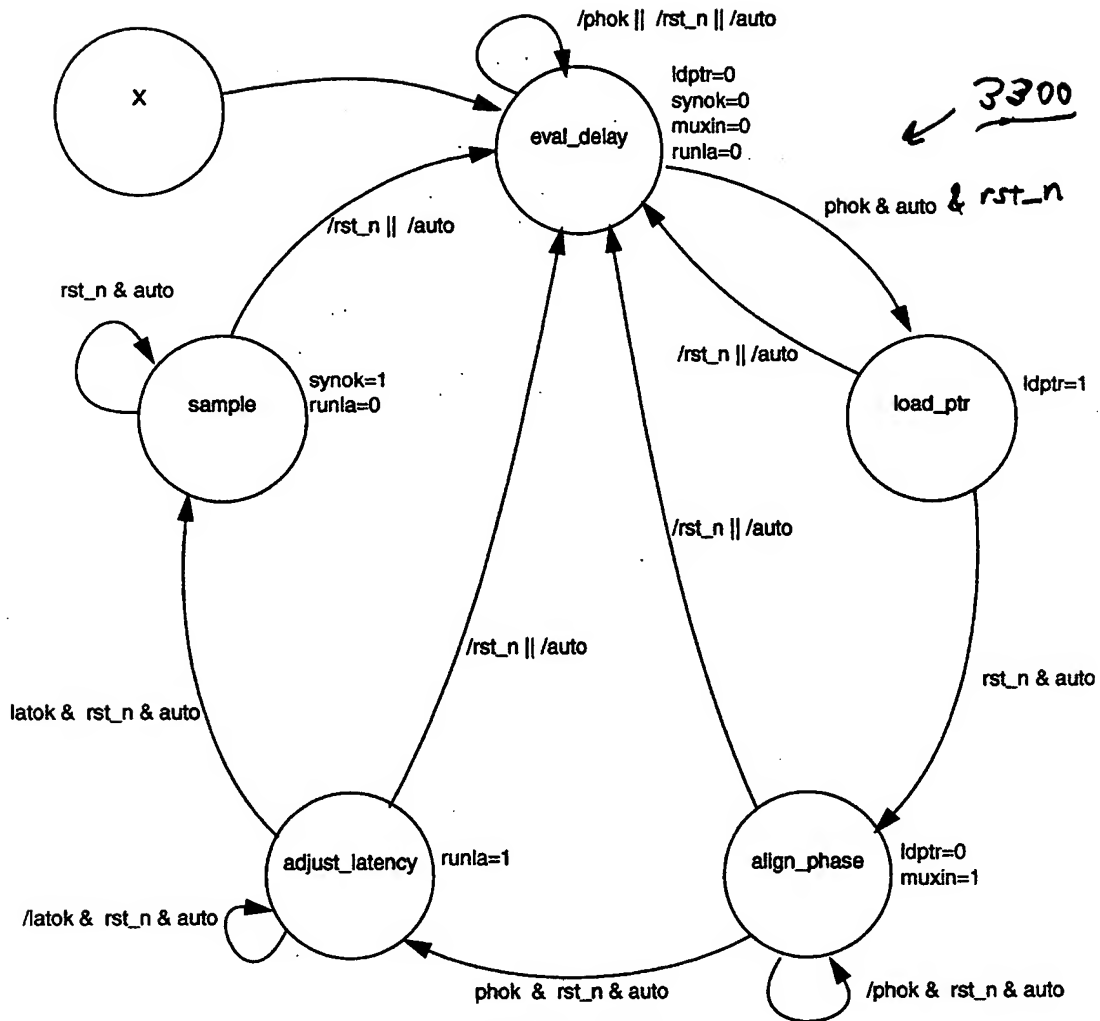


Figure 33

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	FLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR				MUXIN		AUTO

Figure 34

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
XXXXXXXXXX		SYNOK	LATOK	PHOK	FSM_STATE			RLAT			RPTR				

Figure 35

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 36

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	X	0	Expected latency			X	0	X	X	X	X	X	X	X	1

Figure 37

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	1	1	0	0	0	0	0	0	0

Figure 38

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	0	0	0	0	0	0	0

Figure 39

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	0	1	X	X	X	X	X	1	0

Figure 40

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	x	x	x	1	0	0	x	x	x	x	x	0	0

Figure 41

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	Expected latency			1	0	0	x	x	x	x	x	0	0

Figure 42

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	x	x	x	1	0	0	x	x	x	x	x	0	0

Figure 43

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	1	1	1	1	0	0	x	x	x	x	x	0	0

Figure 44